THIN FILM TRANSISTOR ARRAY PANEL FOR LIQUID CRYSTAL DISPLAY

BACKGROUND OF THE INVENTION

(a) Technical Field

The present disclosure relates to a thin film transistor array panel for a liquid crystal display, and in particular, to a thin film transistor array panel including two kinds of field-generating electrodes for generating horizontal electric field.

(b) Description of the Related Art

A conventional liquid crystal display (hereinafter LCD)using horizontal electric field includes pixel electrodes and common electrodes for generating horizontal electric field. An LCD cannot display a high quality image when the behaviors of the liquid crystal molecules are distorted, such as when the common electrodes and a common electrode line connected to the common electrodes for transmitting a common signal are adjacent to each other, generally near a edge portion of a pixel. A wider black matrix may be used to cover the distorted portion of the pixel but it reduces aperture ratio and result in lower brightness of the display.

In addition, cross-talk coupling effect or electric field distortion, which generally occurs between adjacent current carrying lines and electrodes such as between a data signal line and a pixel electrode or a common electrode and a data signal line causes light leakage. Thus, in the conventional technology a common electrode adjacent to the data signal line is made with a width adequate to cover a region of the coupling effect or field distortion. However, the wider coverage reduces the aperture ratio.

Furthermore, since the common electrode or the pixel electrode extend parallel to the data signal line, generally along a longer lengthwise direction of a pixel, the number of electrodes that can be placed thereto is limited.

SUMMARY OF THE INVENTION

It is an aspect of the present invention to provide a high quality image display, minimizing the effect from the distorted electric field of image signal in a liquid crystal display device.

According to one aspect of the present disclosure, a liquid crystal display comprises; a substrate, a first signal line formed on the substrate and extending in a direction, a second signal line intersecting but insulated from the first signal line, a first pixel electrode formed in a pixel area defined by intersections of the first signal line and the second signal line,

said first pixel electrodes substantially parallel to the first signal line, a pixel signal line connected to the pixel electrode, a switching element connected to the first signal line, the second signal line, and the pixel signal line, a first common electrode formed in the pixel area, said first common electrode parallel to said first pixel electrode, a common signal line formed in the pixel area, said common signal line connected to said common electrode, a first capacitor electrode formed in the pixel area, said first capacitor electrode connected to the pixel signal line, a second capacitor electrode formed in the pixel area, said second capacitor electrode connected to said common signal line, a second pixel electrode formed in the pixel area, said second pixel electrode opposite to first pixel electrode with respect to said capacitor electrode and connected to the pixel signal line, and a second common electrode formed in the pixel area, said second common electrode opposite to the first common electrode with respect to said capacitor electrode and connected to the common signal line, wherein said first signal line is curved at near the switching element.

According to another aspect of the present disclosure, a liquid crystal display comprises; a first signal line extending in a direction; a second signal line, said second signal line parallel to the first signal line, a third signal line having a positive angle with respect to a perpendicular direction of the first signal line, said third signal line intersecting the first signal line, a fourth signal line having a negative angle with respect to a

perpendicular direction of the first signal line, said fourth signal line intersecting the first signal line, a pixel area having a first part, a second part and a third part, said pixel area defined by the first, second, third and fourth signal lines, a first common electrode extending parallel to the third signal line, said first common electrode disposed in the first part of the pixel, a first pixel electrode extending parallel to the third signal line, said first pixel electrode disposed in the first part of the pixel area, a second common electrode having a first line and a second line, said first line parallel to the third signal line, said second line parallel to the fourth signal line and said second common electrode disposed in the second part of the pixel area, a second pixel electrode having a third line and a fourth line, said the third line parallel to the third signal line, said fourth line parallel to the fourth signal line and said second pixel electrode disposed in said the second part of the pixel area, a first capacitor electrode electrically connected to the common electrode, said first capacitor electrode disposed in said the second part of the pixel area, a second capacitor electrode electrically connected to the pixel electrode, said second capacitor electrode disposed in said second part of the pixel area, a third common electrode extending parallel to the fourth signal line, said third common electrode disposed in said third part of the pixel area, and a third pixel electrode extending parallel to the fourth signal line, said third pixel electrode disposed in the third part of the pixel area.

The pixel signal line overlaps the common signal line. The common signal line is parallel to the second signal line, which is disposed to the second signal line nearer than the pixel signal line disposed to the switching element. It decreases the effect of electric field distortion arisen from a data signal line and enables to expand transmittable area within the pixel.

The first signal is curved at a positive or negative angle with respect to the perpendicular direction of the second signal line or a rubbing direction on the substrate depending on a polarizing axis. It enables to make a shape of the pixel trapezoid, echelon or others, which also help to decrease or compensate the optical difference of a liquid crystal. The shape of the pixel area may be a rectangular or others.

A storage capacitor formed of the first capacitor electrode and the second capacitor electrode including a insulator interposed, is disposed in the middle of a longitudinal direction of the pixel, or where a texture may be formed during displaying. The capacitor electrode may be a shape of triangle or other.

The first common electrode is disposed nearer to a gate signal line than the first pixel electrode. The second common electrode is also disposed nearer to a gate signal line than the second pixel electrode. It also decrease the effect of electric field distortion arisen from the gate

signal line, which also improve an image quality and enables to expand the transmissible area of the pixel.

The pixel area of the liquid crystal is repeated in a direction of the gate signal line expanding direction, or symmetrically with respect to a data signal line therebetween.

The pixel electrode and the common electrode may be disposed on the same planar place. The common electrode and the pixel electrode may have a thickness of less than about 2000 Å.

The gate line may include a single film of such as Ag, Ag alloy, Al, Al alloy or their alloys. The gate line may also have a multi-layered structure including one of the above-described layers and/ or one of a pad layer.

The pixel electrode and common electrode may be formed of plural parallelism of the two electrodes.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more apparent by describing preferred embodiments thereof in detail with reference to the accompanying drawings in which:

Fig. 1 is a schematic layout view of a thin film transistor (TFT) array panel for an LCD according to a first embodiment of the present invention;

Fig. 2 is a sectional view of the TFT array panel shown in Fig. 1 taken along the line II-II';

Fig. 3 is a sectional view of the TFT array panel shown in Fig. 1 taken along the line III-III'; and

Fig. 4 is a schematic layout view of a TFT array panel for an LCD according to a second embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. The present invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein.

Thin film transistor (TFT) array panels for an LCD according to embodiments of the present invention will be described with reference to the accompanying drawings.

A plurality of gate lines and a plurality of data lines, defining a plurality of pixel areas, are provided on a TFT array panel for an LCD according to the present invention. A plurality of common signal lines, connected to the common electrodes, extend parallel to the data lines or the gate lines. In the absence of electric field liquid crystal molecules are

aligned perpendicular to the data lines or the common signals lines, and the gate lines extend parallel to the common electrodes.

A TFT array panel for an LCD according to a first embodiment of the present invention is now described with reference to Figs. 1-3.

Fig. 1 is a schematic layout view of a pixel in a TFT array panel for an LCD according to a first embodiment of the present invention, and Figs. 2 and 3 are sectional views of the TFT array panel shown in Fig. 1 taken along the lines II-II' and III-III', respectively.

Referring to Figs. 1-3, a plurality of gate lines 121 extending substantially in a transverse direction are formed on an insulating substrate 110. The gate lines 121 may include a single film having low resistivity such as Ag, Ag alloy, Al or Al alloy. The gate lines 121 may also have a multi-layered structure including one of the above-described layers and/or one of a pad layer having good contact characteristics with other materials. An end portion of each gate line 121 transmits a gate signal to the gate line 121 and a plurality of branches of each gate line 121 constitutes a plurality of gate electrodes 123 of TFTs. The gate lines 121 intersect data lines and define a plurality of pixel areas. Preferably, the gate lines are slightly angled at or near the curves of a pixel to form trapezoids.

Furthermore, a plurality of common electrode lines 138 and 132 are formed on the substrate 110. The common electrode lines 138 and 132 extend in a longitudinal direction and parallel to each other. A plurality of

common electrodes 134 connecting the common electrode lines 138 and 132 and extending parallel to the gate lines 121 are also formed on the substrate 110. The common electrodes 134 and the common electrode lines 138 and 132 are disposed at or near the edges of the pixel to form trapezoids. A plurality of first storage capacitor conductors 136, connected to the common electrode lines 138 and 132 or the common electrodes 134 overlap a plurality of second storage capacitor conductors 176 connected to pixel electrodes, forming storage capacitors in a central area of the respective pixel area. The common electrodes 134 and the common electrode lines 138 and 132 are referred to as common signal lines hereinafter. The common electrodes may also be formed symmetrically in a pixel. One half of the common lines may be parallel to a first gate line and a second half of the common lines parallel to a second gate line, the first and second gate lines intersecting each other, as shown in Fig.1 and 4. This structure is applicable to a multi-domain pixel as well as a multi-pixel unit.

A gate insulating layer 140 made of silicon nitride (SiNx) is formed on the gate lines 121 and the common signal lines 132, 134, 136 and 138.

A plurality of semiconductor islands 150 made of hydrogenated amorphous silicon (hereinafter a-Si) are formed on the gate insulating layer 140. A plurality of pairs of ohmic contacts 163 and 165, made of silicide or n+ a-Si heavily doped with n type impurity, are formed on the

semiconductor stripes 151. Each pair of ohmic contacts 163 and 165 are separated with respect to the gate electrodes 123. The semiconductors 150 and the ohmic contacts 163 and 165 may have a linear shape along data lines 171 or may have the same shape as the data lines 171 and drain electrodes 175.

A plurality of data lines 171 and a plurality of drain electrodes 175 are formed on the ohmic contacts 163 and 165 and the gate insulating layer 140. The data lines 171 and the drain electrodes 175 may include a conductive layer having low resistivity such as Al,Ag or its alloy. The data lines 171 extend substantially in the longitudinal direction and intersect the gate lines 121 to define a pixel area in various shapes such as an echelon rectangular, trapezoidal, etc. A plurality of branches of each data line 171 extend onto the ohmic contacts 163 to form a plurality of TFT source electrodes 173. An end portion (not shown) of each data line 171 transmits image signals to the data lines 171. The drain electrodes 175 are separated from the data lines 171 and located on the ohmic contacts 165 opposite the source electrodes 173 with respect to the gate electrodes 123.

According to a preferred embodiment of the invention, a plurality of pixel electrodes 174, a plurality of pixel electrode lines 172 and 178, and a plurality of second storage capacitor conductors 176 are formed on the gate insulating layer 140. The pixel electrodes 174 extend opposite the

common electrodes 134. The pixel electrode lines 172 and 178 are connected to the drain electrodes 175 and located near the edges of the pixel areas and overlap the common electrode lines 132 and 138. The second storage capacitor conductors 176 are connected to the pixel electrode lines 172 and overlap the first storage capacitor conductors 136 to form storage capacitors. The pixel electrodes 174 and the pixel electrode lines 172 and 178 are referred to as a pixel signal lines hereinafter.

A passivation layer 180 is formed on the data lines 171, the drain electrodes 175, the pixel signal lines 172, 174 and 178, and the exposed portions of the semiconductor islands 150. The passivation layer 180 is preferably made of silicon nitride or organic material having a good flatness characteristic.

An alignment layer 11 for aligning liquid crystal molecules is formed on the passivation layer 180.

A gate electrode 123, a source electrode 173, and a drain electrode 175 along with a semiconductor island 154 and a pair of ohmic contacts 163 and 165 form a TFT.

Although the common signal lines 132, 134 and 138 and the pixel signal lines 172, 174 and 178 are formed of the same layer as the gate lines 121 and the data lines 171, respectively, they may be on the same layer, for example, they may be located on the passivation layer 180. The

common signal lines 132, 134 and 138 and the pixel signal lines 172, 174 and 178 preferably have thickness equal to or less than about 2,000 Å. This thickness presents alignment defect due to height difference.

Transverse arrows shown in Fig. 1 indicate a rubbing direction at the alignment layer 11 which is perpendicular to the data lines 171 or the common signal lines 132. The rubbing direction can be in directions other than that shown by the arrows.

In a TFT array panel for an LCD according to the first embodiment the common signal lines 132 extend parallel to the data lines 171 along long edges of the pixel areas. The rubbing direction is also determined such that in absence of electric field the liquid crystal molecules are aligned perpendicular to the data lines 171 . Accordingly, an electric field generated by the voltage difference between the data lines 171 and the common signal lines 132 orients the liquid crystal molecules to their initial orientations. The corresponding areas are displayed dark to prevent lateral crosstalk. As a result, the common signal lines 132 can be made to have a small width and aperture ratio can be increased.

In addition, since the common electrodes 134 and the pixel electrodes 174 are arranged along a long edge direction of the pixel areas the number of the electrodes 134 and 174 and their positioning can be easily varied.

Furthermore, the effective display area can be enlarged to corners of the pixel areas because the pixel electrodes 174 or the common electrodes 134 located near the edges of the pixel areas extend parallel to the edges of the pixel areas defined by the gate lines 121 and the data lines 171. Moreover, the storage capacitors are located near the centers of the pixel area, where textures are generated so that they do not reduce the transmittance of the pixel areas, thereby maximizing the transmittance of the pixel areas.

Although the above-described first embodiment arranges two adjacent trapezoidal pixel electrodes in a row such that bottom edges or top edges of the trapezoids face each other as shown in Figs. 1 to 3, a bottom edge of a pixel area may face a top edge of an adjacent pixel area in the row direction and vice versa, which is now described with reference to Figure 4.

Fig. 4 is a layout view of a TFT array panel for an LCD according to a second embodiment. The section view of the TFT array panel according to the second embodiment is similar to that of the first embodiment of the present invention.

The pixel areas, however, are repeatedly arranged in a row direction. That is, the adjacent pixel areas in a pixel row have the same shape, while those shown in Fig. 1 have inverted or reversed shapes such that they are symmetrical with respect to a data line located therebetween.

As described above, the placement of the common signal lines and the data in parallel along edges of the pixel areas and reduces light leakage. In addition, the parallelism between the common electrodes and the pixel electrodes or edges of the trapezoidal pixel areas extends display to the corners of the pixel areas, thereby maximizing display capacity of pixels. Moreover, the arrangement of the common electrodes and the pixel electrodes along a long edge direction of the pixels facilitates to a more varied placement the electrodes increases the aperture ratio.

While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.